

# MC145170-1

## Advance Information PLL Frequency Synthesizer with Serial Interface CMOS

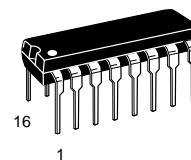
The new MC145170-1 is pin-for-pin compatible with the MC145170. A comparison of the two parts is shown in the table below. The MC145170-1 is recommended for new designs.

The MC145170-1 is a single-chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL the easiest to program in the industry. Either a bit- or byte-oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2-byte serial transfer to the 16-bit N register.

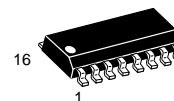
The device features fully programmable R and N counters, an amplifier at the  $f_{in}$  pin, on-chip support of an external crystal, a programmable reference output, and both single- and double-ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam-load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam-loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

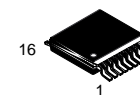
- Operating Voltage Range: 2.5 to 5.5 V
- Maximum Operating Frequency:
  - 185 MHz @  $V_{in} = 500$  mV p-p, 4.5 V Minimum Supply
  - 100 MHz @  $V_{in} = 500$  mV p-p, 3.0 V Minimum Supply
- Operating Supply Current:
  - 0.6 mA @ 3 V, 30 MHz
  - 1.5 mA @ 3 V, 100 MHz
  - 3.0 mA @ 5 V, 50 MHz
  - 5.8 mA @ 5 V, 185 MHz
- Operating Temperature Range: -40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI and National MICROWIRE™ Serial Data Ports
- Chip Complexity: 4800 FETs or 1200 Equivalent Gates
- See Application Note AN1207/D



**P SUFFIX**  
PLASTIC DIP  
CASE 648



**D SUFFIX**  
SOG PACKAGE  
CASE 751B

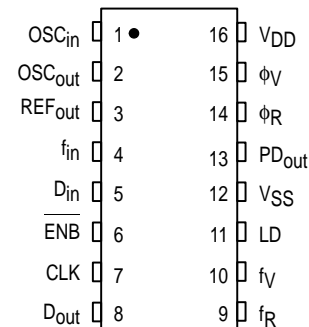


**DT SUFFIX**  
TSSOP  
CASE 948C

### ORDERING INFORMATION

MC145170P1 Plastic DIP  
MC145170D1 SOG Package  
MC145170DT1 TSSOP

### PIN ASSIGNMENT



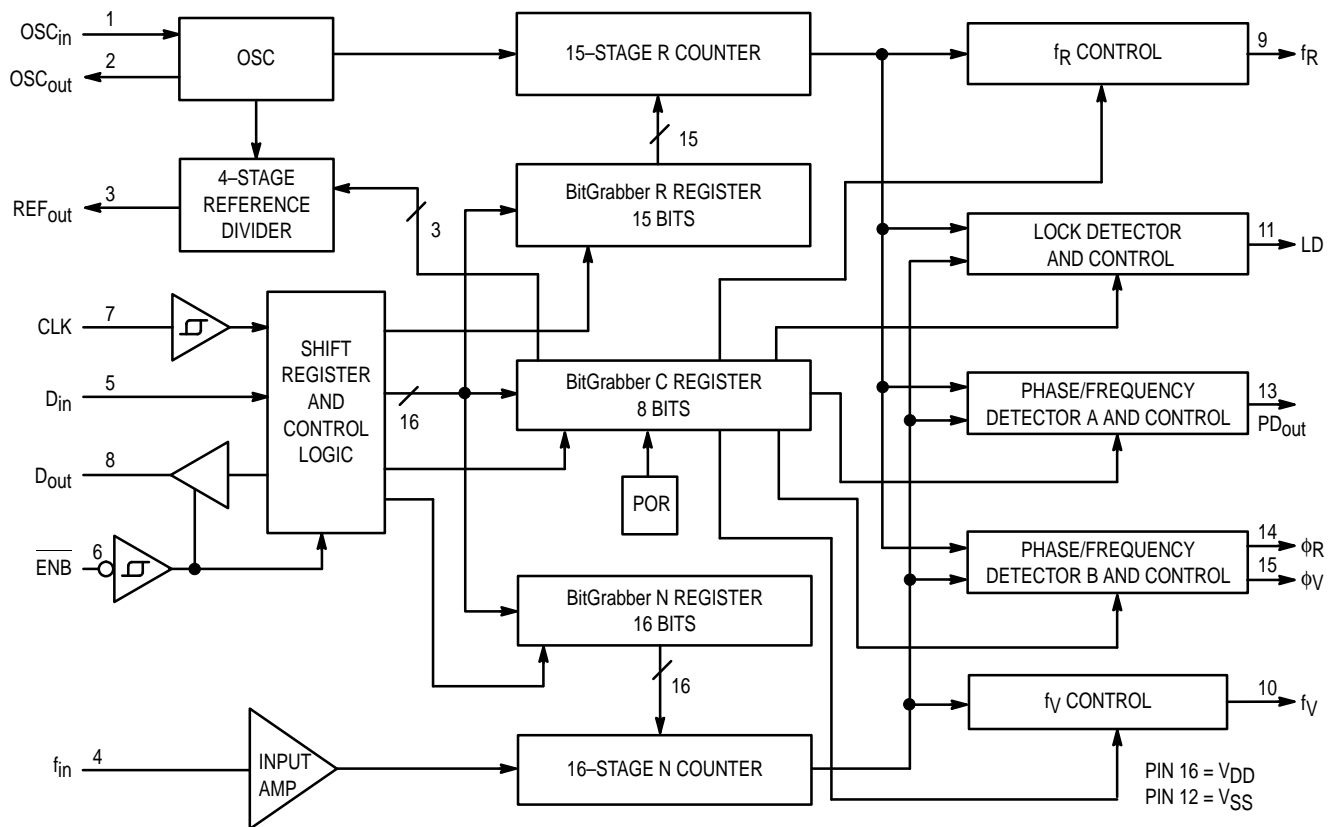
### COMPARISON OF THE PLL FREQUENCY SYNTHESIZERS

Parameter	MC145170-1	MC145170
Technology	1.2 μm CMOS	1.5 μm CMOS
Maximum Frequency with 5 V ± 10% Supply, f <sub>in</sub>	185 MHz	160 MHz
Maximum Frequency with 5 V ± 10% Supply, OSC <sub>in</sub>	25 MHz	20 MHz
Maximum Supply Voltage	5.5 V	6.0 V
Maximum Input Capacitance, f <sub>in</sub>	7 pF	5 pF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BitGrabber is a trademark of Motorola Inc. MICROWIRE is a trademark of National Semiconductor Corp.

## BLOCK DIAGRAM



### MAXIMUM RATINGS\* (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to + 5.5	V
$V_{in}$	DC Input Voltage	- 0.5 to $V_{DD} + 0.5$	V
$V_{out}$	DC Output Voltage	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 10$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 20$	mA
$I_{DD}$	DC Supply Current, $V_{DD}$ and $V_{SS}$ Pins	$\pm 30$	mA
$P_D$	Power Dissipation, per Package	300	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	$^{\circ}C$
$T_L$	Lead Temperature, 1 mm from Case for 10 seconds	260	$^{\circ}C$

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ ,  $T_A = -40$  to  $+85^\circ\text{C}$ )

Symbol	Parameter	Test Condition	$V_{DD}$ V	Guaranteed Limit	Unit
$V_{DD}$	Power Supply Voltage Range		—	2.5 to 5.5	V
$V_{IL}$	Maximum Low-Level Input Voltage* ( $D_{in}$ , CLK, ENB, $f_{in}$ )	dc Coupling to $f_{in}$	2.5 4.5 5.5	0.50 1.35 1.65	V
$V_{IH}$	Minimum High-Level Input Voltage* ( $D_{in}$ , CLK, ENB, $f_{in}$ )	dc Coupling to $f_{in}$	2.5 4.5 5.5	2.00 3.15 3.85	V
$V_{Hys}$	Minimum Hysteresis Voltage (CLK, ENB)		2.5 5.5	0.15 0.20	V
$V_{OL}$	Maximum Low-Level Output Voltage (Any Output)	$I_{out} = 20 \mu\text{A}$	2.5 5.5	0.1 0.1	V
$V_{OH}$	Minimum High-Level Output Voltage (Any Output)	$I_{out} = -20 \mu\text{A}$	2.5 5.5	2.4 5.4	V
$I_{OL}$	Minimum Low-Level Output Current ( $PD_{out}$ , $REF_{out}$ , $f_R$ , $f_V$ , LD, $\phi_R$ , $\phi_V$ )	$V_{out} = 0.3 \text{ V}$ $V_{out} = 0.4 \text{ V}$ $V_{out} = 0.5 \text{ V}$	2.5 4.5 5.5	0.12 0.36 0.36	mA
$I_{OH}$	Minimum High-Level Output Current ( $PD_{out}$ , $REF_{out}$ , $f_R$ , $f_V$ , LD, $\phi_R$ , $\phi_V$ )	$V_{out} = 2.2 \text{ V}$ $V_{out} = 4.1 \text{ V}$ $V_{out} = 5.0 \text{ V}$	2.5 4.5 5.5	-0.12 -0.36 -0.36	mA
$I_{OL}$	Minimum Low-Level Output Current ( $D_{out}$ )	$V_{out} = 0.4 \text{ V}$	4.5	1.6	mA
$I_{OH}$	Minimum High-Level Output Current ( $D_{out}$ )	$V_{out} = 4.1 \text{ V}$	4.5	-1.6	mA
$I_{in}$	Maximum Input Leakage Current ( $D_{in}$ , CLK, ENB, $OSC_{in}$ )	$V_{in} = V_{DD}$ or $V_{SS}$	5.5	$\pm 1.0$	$\mu\text{A}$
$I_{in}$	Maximum Input Current ( $f_{in}$ )	$V_{in} = V_{DD}$ or $V_{SS}$	5.5	$\pm 120$	$\mu\text{A}$
$I_{OZ}$	Maximum Output Leakage Current ( $PD_{out}$ )  ( $D_{out}$ )	$V_{in} = V_{DD}$ or $V_{SS}$ , Output in High-Impedance State	5.5  5.5	$\pm 100$  $\pm 5$	nA  $\mu\text{A}$
$I_{DD}$	Maximum Quiescent Supply Current	$V_{in} = V_{DD}$ or $V_{SS}$ ; Outputs Open; Excluding $f_{in}$ Amp Input Current Component	5.5	100	$\mu\text{A}$
$I_{dd}$	Maximum Operating Supply Current	$f_{in} = 500 \text{ mV p-p}$ ; $OSC_{in} = 1 \text{ MHz @ } 1 \text{ V p-p}$ ; LD, $f_R$ , $f_V$ , $REF_{out} = \text{Inactive and No Connect}$ ; $OSC_{out}$ , $\phi_V$ , $\phi_R$ , $PD_{out} = \text{No Connect}$ ; $D_{in}$ , ENB, CLK = $V_{DD}$ or $V_{SS}$	—	**	mA

\* When dc coupling to the  $OSC_{in}$  pin is used, the pin must be driven rail-to-rail. In this case,  $OSC_{out}$  should be floated.

\*\* The nominal values at 3 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

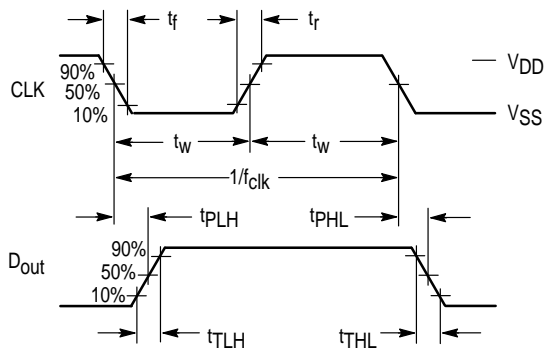
**AC INTERFACE CHARACTERISTICS** (  $T_A = -40$  to  $+85^\circ\text{C}$ ,  $C_L = 50$  pF, Input  $t_r = t_f = 10$  ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V <sub>DD</sub> V	Guaranteed Limit	Unit
$f_{\text{clk}}$	Serial Data Clock Frequency (Note: Refer to Clock $t_w$ Below)	1	2.5 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay, CLK to D <sub>Out</sub>	1, 5	2.5 4.5 5.5	150 85 85	ns
$t_{\text{PLZ}}$ , $t_{\text{PHZ}}$	Maximum Disable Time, D <sub>Out</sub> Active to High Impedance	2, 6	2.5 4.5 5.5	300 200 200	ns
$t_{\text{PZL}}$ , $t_{\text{PZH}}$	Access Time, D <sub>Out</sub> High Impedance to Active	2, 6	2.5 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
$t_{\text{TLH}}$ , $t_{\text{THL}}$	Maximum Output Transition Time, D <sub>Out</sub> <span style="float:right">CL = 50 pF</span>	1, 5	2.5	150	ns
			4.5	50	
	<span style="float:right">CL = 200 pF</span>	1, 5	2.5	900	ns
			4.5	150	
			5.5	150	
$C_{\text{in}}$	Maximum Input Capacitance – D <sub>in</sub> , ENB, CLK		—	10	pF
$C_{\text{out}}$	Maximum Output Capacitance – D <sub>Out</sub>		—	10	pF

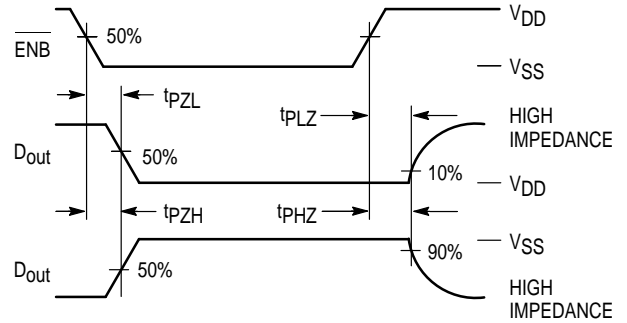
**TIMING REQUIREMENTS** (  $T_A = -40$  to  $+85^\circ\text{C}$ , Input  $t_r = t_f = 10$  ns unless otherwise indicated)

Symbol	Parameter	Figure No.	V <sub>DD</sub> V	Guaranteed Limit	Unit
$t_{\text{su}}$ , $t_{\text{h}}$	Minimum Setup and Hold Times, D <sub>in</sub> vs CLK	3	2.5 4.5 5.5	55 40 40	ns
$t_{\text{su}}$ , $t_{\text{h}}$ , $t_{\text{rec}}$	Minimum Setup, Hold, and Recovery Times, ENB vs CLK	4	2.5 4.5 5.5	135 100 100	ns
$t_{\text{w(H)}}$	Minimum Inactive–High Pulse Width, ENB	4	2.5 4.5 5.5	400 300 300	ns
$t_{\text{w}}$	Minimum Pulse Width, CLK	1	2.5 4.5 5.5	166 125 125	ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Times, CLK	1	2.5 4.5 5.5	100 100 100	μs

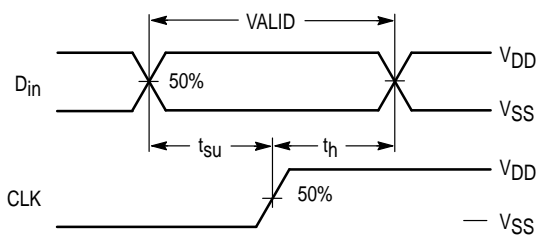
## SWITCHING WAVEFORMS



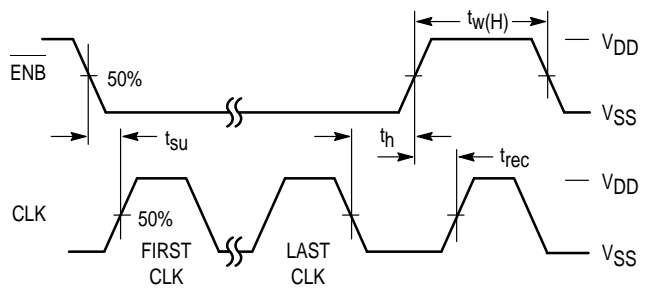
**Figure 1.**



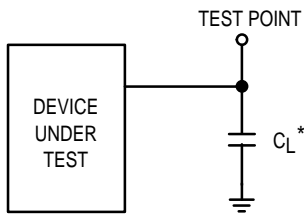
**Figure 2.**



**Figure 3.**

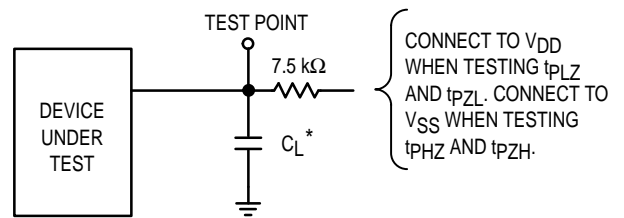


**Figure 4.**



\* Includes all probe and fixture capacitance.

**Figure 5. Test Circuit**



CONNECT TO  $V_{DD}$  WHEN TESTING  $t_{PLZ}$  AND  $t_{PZL}$ . CONNECT TO  $V_{SS}$  WHEN TESTING  $t_{PHZ}$  AND  $t_{PZH}$ .

\* Includes all probe and fixture capacitance.

**Figure 6. Test Circuit**

**LOOP SPECIFICATIONS** (  $T_A = -40$  to  $+85^\circ\text{C}$  )

Symbol	Parameter	Test Condition	Figure No.	V <sub>DD</sub> V	Guaranteed Range		Unit
					Min	Max	
f	Input Frequency, $f_{in}$	$V_{in} \geq 500$ mV p-p Sine Wave, N Counter Set to Divide Ratio Such that $f_V \leq 2$ MHz	7	2.5 3.0 4.5 5.5	5* 5* 25* 45*	TBD 100 185 185	MHz
f	Input Frequency, OSC <sub>in</sub> Externally Driven with ac-Coupled Signal	$V_{in} \geq 1$ V p-p Sine Wave, OSC <sub>out</sub> = No Connect, R Counter Set to Divide Ratio Such that $f_R \leq 2$ MHz	8	2.5 3.0 4.5 5.5	1* 1* 1* 1*	12 14 25 25	MHz
f <sub>X TAL</sub>	Crystal Frequency, OSC <sub>in</sub> and OSC <sub>out</sub>	$C_1 \leq 30$ pF $C_2 \leq 30$ pF Includes Stray Capacitance	9	2.5 3.0 4.5 5.5	2 2 2 2	12 12 15 15	MHz
f <sub>out</sub>	Output Frequency, REF <sub>out</sub>	$C_L = 30$ pF	10, 12	2.5 4.5 5.5	dc dc dc	TBD 10 10	MHz
f	Operating Frequency of the Phase Detectors			2.5 4.5 5.5	dc dc dc	TBD 2 2	MHz
t <sub>w</sub>	Output Pulse Width, $\phi_R$ , $\phi_V$ , and LD	$f_R$ in Phase with $f_V$ $C_L = 50$ pF	11, 12	2.5 4.5 5.5	TBD 20 16	TBD 100 90	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Output Transition Times, $\phi_R$ , $\phi_V$ , LD, $f_R$ , and $f_V$	$C_L = 50$ pF	11, 12	2.5 4.5 5.5	— — —	TBD 65 60	ns
C <sub>in</sub>	Input Capacitance	$f_{in}$ OSC <sub>in</sub>	— —	— —	— —	7 7	pF

\* If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac-coupled case. Also, see Figure 22 for dc decoupling.

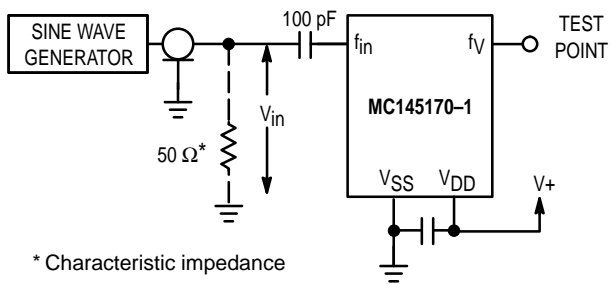


Figure 7. Test Circuit

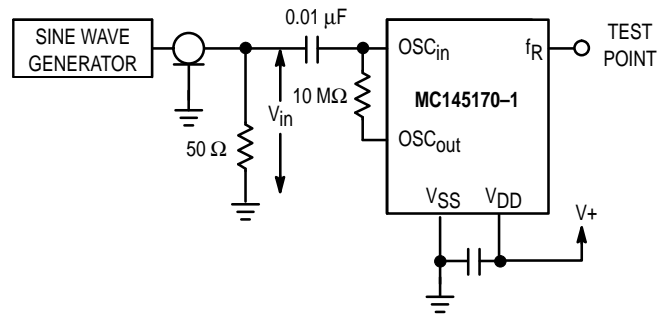


Figure 8. Test Circuit

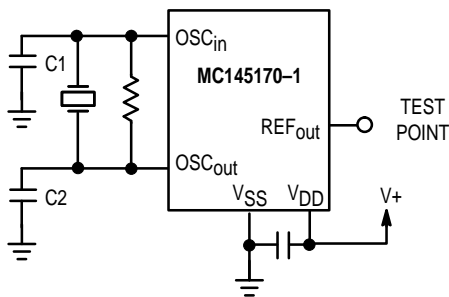


Figure 9. Test Circuit

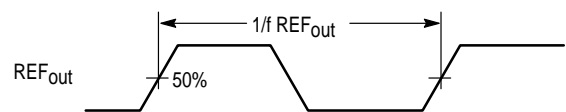


Figure 10. Switching Waveform

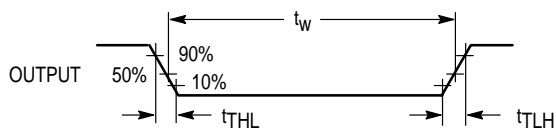


Figure 11. Switching Waveform

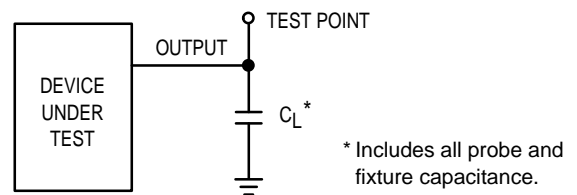


Figure 12. Test Circuit

## PIN DESCRIPTIONS

### DIGITAL INTERFACE PINS

#### D<sub>in</sub>

#### Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low-to-high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15-bit transfer (see Table 1). An optional pattern which resets the device is shown in Figure 13. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by ENB.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.5 to 5.5 V. The formats are shown in Figures 13, 14, 15, and 16.

D<sub>in</sub> typically switches near 50% of V<sub>DD</sub> to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I<sub>OL</sub> of the driving device, maximum tolerable power consumption, and maximum data rate.

**Table 1. Register Access**  
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
4 + 5	(Reset)	
8	C Register	C7, C6, C5, . . . , C0
16	N Register	N15, N14, N13, . . . , N0
15 or 24	R Register	R14, R13, R12, . . . , R0
Other Values ≤ 32	None	
Values > 32	See Figures 24 — 31	

#### CLK

#### Serial Data Clock Input (Pin 7)

Low-to-high transitions on Clock shift bits available at D<sub>in</sub>, while high-to-low transitions shift bits from D<sub>out</sub>. The chip's 16-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, 15, and 16). For cascaded devices, see Figures 24 — 31.

CLK typically switches near 50% of V<sub>DD</sub> and has a Schmitt-triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of D<sub>in</sub> for more information.

#### NOTE

To guarantee proper operation of the power-on reset (POR) circuit, the CLK pin must be held at the potential of either the V<sub>SS</sub> or V<sub>DD</sub> pin during power up. That is, the CLK input should not be floated or toggled while the V<sub>DD</sub> pin is ramping from 0 to at least 2.5 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 13 must be used.

#### ENB

#### Active-Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When ENB is in an inactive high state, shifting is inhibited, D<sub>out</sub> is forced to the high-impedance state, and the port is held in the initialized state. To transfer data to the device, ENB (which must start inactive high) is taken low, a serial transfer is made via D<sub>in</sub> and CLK, and ENB is taken back high. The low-to-high transition on ENB transfers data to the C, N, or R register depending on the data stream length per Table 1.

#### NOTE

Transitions on ENB must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when ENB is high and CLK is low.

This input is also Schmitt-triggered and switches near 50% of V<sub>DD</sub>, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of D<sub>in</sub> for more information.

#### D<sub>out</sub>

#### Three-State Serial Data Output (Pin 8)

Data is transferred out of the 16-1/2-stage shift register through D<sub>out</sub> on the high-to-low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D<sub>out</sub> could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in-line QA test during board manufacturing.

Finally, D<sub>out</sub> facilitates troubleshooting a system and permits cascading devices.

### REFERENCE PINS

#### OSC<sub>in</sub>/OSC<sub>out</sub>

#### Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.



If desired, an external clock source can be ac coupled to OSC<sub>in</sub>. A 0.01 μF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. An external feedback resistor of approximately 10 MΩ is required across the OSC<sub>in</sub> and OSC<sub>out</sub> pins in the ac-coupled case (see Figure 8). *OSC<sub>out</sub> is an internal node on the device and should not be used to drive any loads* (i.e., OSC<sub>out</sub> is unbuffered). However, the buffered REF<sub>out</sub> is available to drive external loads.

The external signal level must be at least 1 V p-p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings rail-to-rail (V<sub>DD</sub> to V<sub>SS</sub>), then dc coupling can be used. In the dc-coupled case, no external feedback resistor is needed. OSC<sub>out</sub> must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC<sub>in</sub> pin. See Figure 22.

Each rising edge on the OSC<sub>in</sub> pin causes the R counter to decrement by one.

#### REF<sub>out</sub> Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal-generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 14).

REF<sub>out</sub> can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on-chip power-on-initialize circuit forces REF<sub>out</sub> to the OSC<sub>in</sub> divided-by-8 mode.

REF<sub>out</sub> is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC<sub>in</sub> frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

### COUNTER OUTPUT PINS

#### f<sub>R</sub> R Counter Output (Pin 9)

This signal is the buffered output of the 15-stage R counter. f<sub>R</sub> can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f<sub>R</sub> signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC<sub>in</sub> pin is allowed by choosing a divide value of 1 (see Figure 15). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f<sub>R</sub> must not exceed 2 MHz.

When activated, the f<sub>R</sub> signal appears as normally low and pulses high.

#### f<sub>V</sub> N Counter Output (Pin 10)

This signal is the buffered output of the 16-stage N counter. f<sub>V</sub> can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f<sub>V</sub> signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f<sub>V</sub> must not exceed 2 MHz.

When activated, the f<sub>V</sub> signal appears as normally low and pulses high.

### LOOP PINS

#### f<sub>in</sub> Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on-chip amplifier which drives the N counter. This signal is normally sourced from an external voltage-controlled oscillator (VCO), and is ac-coupled into f<sub>in</sub>. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V<sub>IL</sub> to V<sub>IH</sub> levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f<sub>in</sub> pin. See Figure 22.

Each rising edge on the f<sub>in</sub> pin causes the N counter to decrement by 1.

#### PD<sub>out</sub> Single-Ended Phase/Frequency Detector Output (Pin 13)

This is a three-state output for use as a loop error signal when combined with an external low-pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of f<sub>V</sub> > f<sub>R</sub> or Phase of f<sub>V</sub> Leading f<sub>R</sub>: negative pulses from high impedance

Frequency of f<sub>V</sub> < f<sub>R</sub> or Phase of f<sub>V</sub> Lagging f<sub>R</sub>: positive pulses from high impedance

Frequency and Phase of f<sub>V</sub> = f<sub>R</sub>: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of f<sub>V</sub> > f<sub>R</sub> or Phase of f<sub>V</sub> Leading f<sub>R</sub>: positive pulses from high impedance

Frequency of f<sub>V</sub> < f<sub>R</sub> or Phase of f<sub>V</sub> Lagging f<sub>R</sub>: negative pulses from high impedance

Frequency and Phase of f<sub>V</sub> = f<sub>R</sub>: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD<sub>OUT</sub> can be forced to the high-impedance state by utilization of the disable feature in the C register (patented).

**$\phi_R$  and  $\phi_V$   
Double-Ended Phase/Frequency Detector Outputs  
(Pins 14, 15)**

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of  $f_V > f_R$  or Phase of  $f_V$  Leading  $f_R$ :  $\phi_V$  = negative pulses,  $\phi_R$  = essentially high

Frequency of  $f_V < f_R$  or Phase of  $f_V$  Lagging  $f_R$ :  $\phi_V$  = essentially high,  $\phi_R$  = negative pulses

Frequency and Phase of  $f_V = f_R$ :  $\phi_V$  and  $\phi_R$  remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of  $f_V > f_R$  or Phase of  $f_V$  Leading  $f_R$ :  $\phi_R$  = negative pulses,  $\phi_V$  = essentially high

Frequency of  $f_V < f_R$  or Phase of  $f_V$  Lagging  $f_R$ :  $\phi_R$  = essentially high,  $\phi_V$  = negative pulses

Frequency and Phase of  $f_V = f_R$ :  $\phi_V$  and  $\phi_R$  remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

**LD  
Lock Detector Output (Pin 11)**

This output is essentially at a high level with narrow low-going pulses when the loop is locked ( $f_R$  and  $f_V$  of the same phase and frequency). The output pulses low when  $f_V$  and  $f_R$  are out of phase or different frequencies (see Figure 17).

This output can be enabled and disabled via the C register (patented). Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

**POWER SUPPLY**

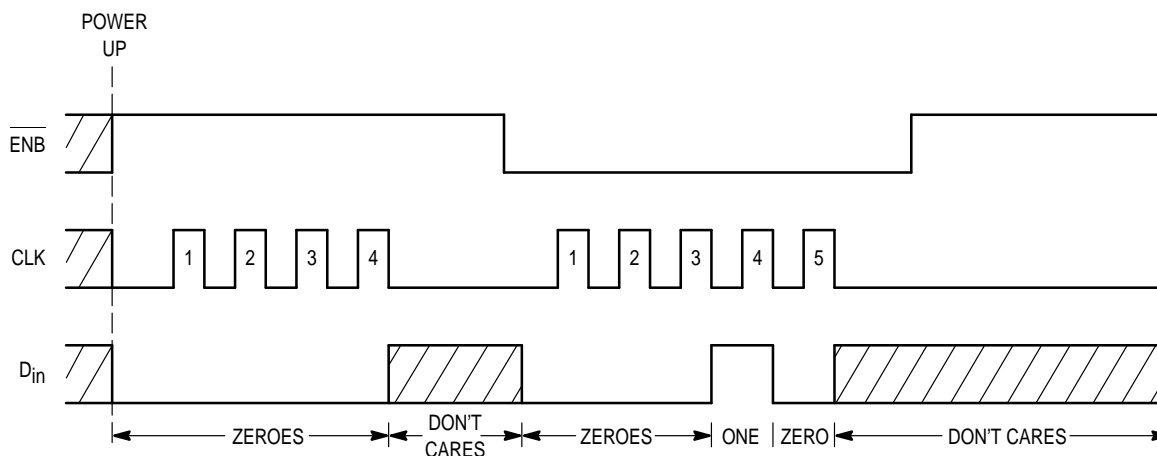
**V<sub>DD</sub>  
Most Positive Supply Potential (Pin 16)**

This pin may range from + 2.5 to 5.5 V with respect to V<sub>SS</sub>.

For optimum performance, V<sub>DD</sub> should be bypassed to V<sub>SS</sub> using low-inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

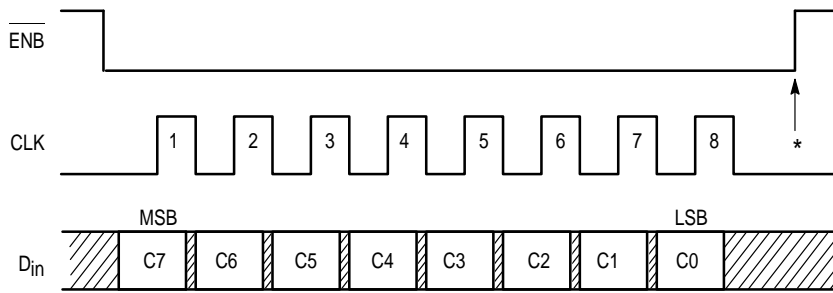
**V<sub>SS</sub>  
Most Negative Supply Potential (Pin 12)**

This pin is usually ground. For measurement purposes, the V<sub>SS</sub> pin is tied to a ground plane.



NOTE: This initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (pin 7) toggles or floats upon power up, use the above sequence to reset the device. Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.5 V, but not down to 0 V (for example, the supply drops down to 1 V). This is necessary because the on-chip power-on reset is only activated when the supply ramps up from 0 V.

Figure 13. Reset Sequence



\* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

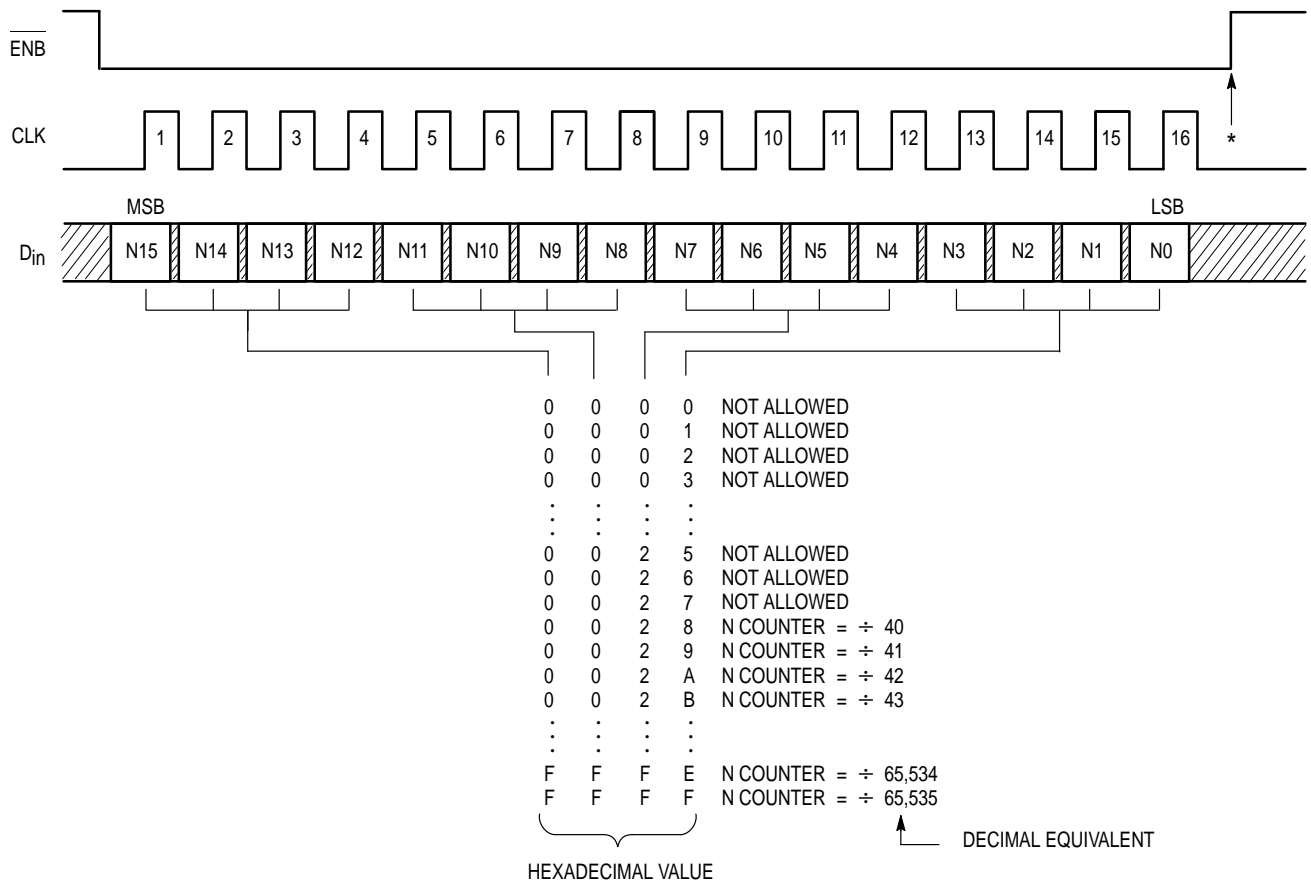
- C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD<sub>out</sub> and interchanges the  $\phi_R$  function with  $\phi_V$  as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.
- C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD<sub>out</sub>) and disables phase/frequency detector B by forcing  $\phi_R$  and  $\phi_V$  to the static high state. When cleared low, phase/frequency detector B is enabled ( $\phi_R$  and  $\phi_V$ ) and phase/frequency detector A is disabled with PD<sub>out</sub> forced to the high-impedance state. This bit is cleared low at power up.
- C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.
- C4 – C2, OSC2 – OSC0: Reference output controls which determine the REF<sub>out</sub> characteristics as shown below. Upon power up, the bits are initialized such that OSC<sub>in</sub>/8 is selected.

C4	C3	C2	REF <sub>out</sub> Frequency
0	0	0	dc (Static Low)
0	0	1	OSC <sub>in</sub>
0	1	0	OSC <sub>in</sub> /2
0	1	1	OSC <sub>in</sub> /4
1	0	0	OSC <sub>in</sub> /8
1	0	1	OSC <sub>in</sub> /16
1	1	0	OSC <sub>in</sub> /8
1	1	1	OSC <sub>in</sub> /16

- C1 — f<sub>V</sub>E: Enables the f<sub>V</sub> output when set high. When cleared low, the f<sub>V</sub> output is forced to a static low level. The bit is cleared low upon power up.
- C0 — f<sub>R</sub>E: Enables the f<sub>R</sub> output when set high. When cleared low, the f<sub>R</sub> output is forced to a static low level. The bit is cleared low upon power up.

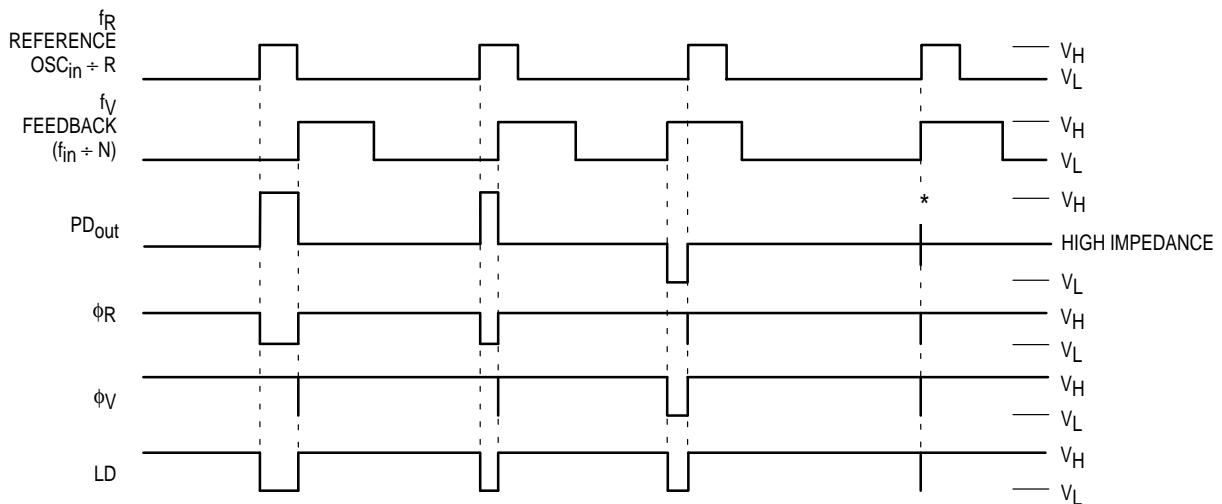
**Figure 14. C Register Access and Format (8 Clock Cycles are Used)**





\* At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam-loaded and begin counting down together.

**Figure 16. N Register Access and Format (16 Clock Cycles Are Used)**



$V_H$  = High voltage level  
 $V_L$  = Low voltage level

\*At this point, when both  $f_R$  and  $f_V$  are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.

NOTE: The  $PD_{out}$  generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor.  $PD_{out}$ ,  $\phi_R$ , and  $\phi_V$  are shown with the polarity bit (POL) = low; see Figure 14 for POL.

**Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms**

## DESIGN CONSIDERATIONS

### CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

#### Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC<sub>in</sub>. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC<sub>in</sub> may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

#### Design an Off-Chip Reference

The user may design an off-chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC<sub>in</sub> (see Figure 18). For large amplitude signals (standard CMOS logic levels), dc coupling is used.

#### Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C<sub>L</sub>) which does not exceed 20 pF when used at the highest operating frequencies listed in the **Loop Specifications** table. Larger C<sub>L</sub> values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C<sub>L</sub>) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C_1 \cdot C_2}{C_1 + C_2}$$

where

C<sub>in</sub> = 5 pF (see Figure 19)

C<sub>out</sub> = 6 pF (see Figure 19)

C<sub>a</sub> = 1 pF (see Figure 19)

C<sub>1</sub> and C<sub>2</sub> = external capacitors (see Figure 18)

C<sub>stray</sub> = the total equivalent external circuit stray capacitance appearing across the crystal terminals

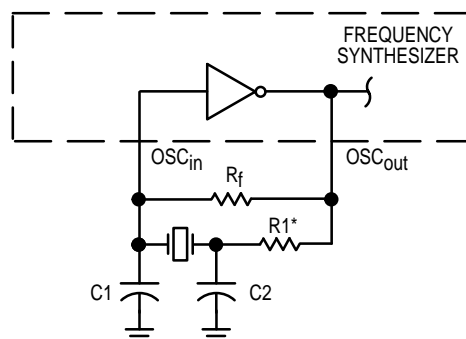
The oscillator can be "trimmed" on-frequency by making a portion or all of C<sub>1</sub> variable. The crystal and associated components must be located as close as possible to the OSC<sub>in</sub> and OSC<sub>out</sub> pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C<sub>in</sub> and C<sub>out</sub>. For this approach, the term C<sub>stray</sub> becomes 0 in the above expression for C<sub>L</sub>.

Power is dissipated in the effective series resistance of the crystal, R<sub>e</sub>, in Figure 20. The maximum drive level specified

by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF<sub>out</sub> pin (OSC<sub>out</sub> is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).



\* May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

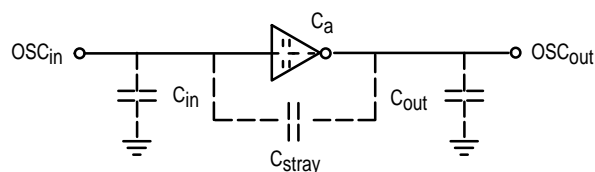
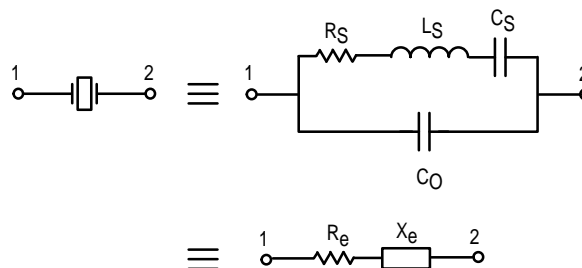


Figure 19. Parasitic Capacitances of the Amplifier and C<sub>stray</sub>



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

## RECOMMENDED READING

Technical Note TN-24, Statek Corp.  
Technical Note TN-7, Statek Corp.  
E. Hafner, "The Piezoelectric Crystal Unit-Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

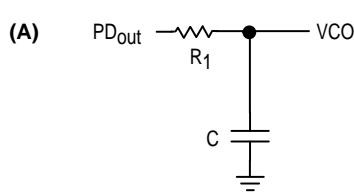
D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

**Table 2. Partial List of Crystal Manufacturers**

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693-0099

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

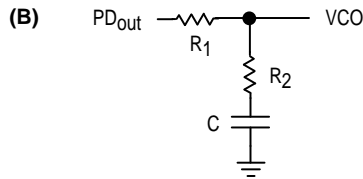
## PHASE-LOCKED LOOP — LOW PASS FILTER DESIGN



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

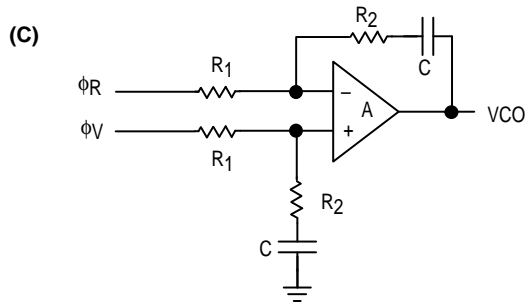
$$F(s) = \frac{1}{R_1sC + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5 \omega_n \left( R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

**NOTE:**

For (C),  $R_1$  is frequently split into two series resistors; each resistor is equal to  $R_1$  divided by 2. A capacitor  $C_C$  is then placed from the midpoint to ground to further filter the error pulses. The value of  $C_C$  should be such that the corner frequency of this network does not significantly affect  $\omega_n$ .

**DEFINITIONS:**

- N = Total Division Ratio in Feedback Loop
- $K_\phi$  (Phase Detector Gain) =  $V_{DD} / 4\pi$  V/radian for  $PD_{out}$
- $K_\phi$  (Phase Detector Gain) =  $V_{DD} / 2\pi$  V/radian for  $\phi_V$  and  $\phi_R$

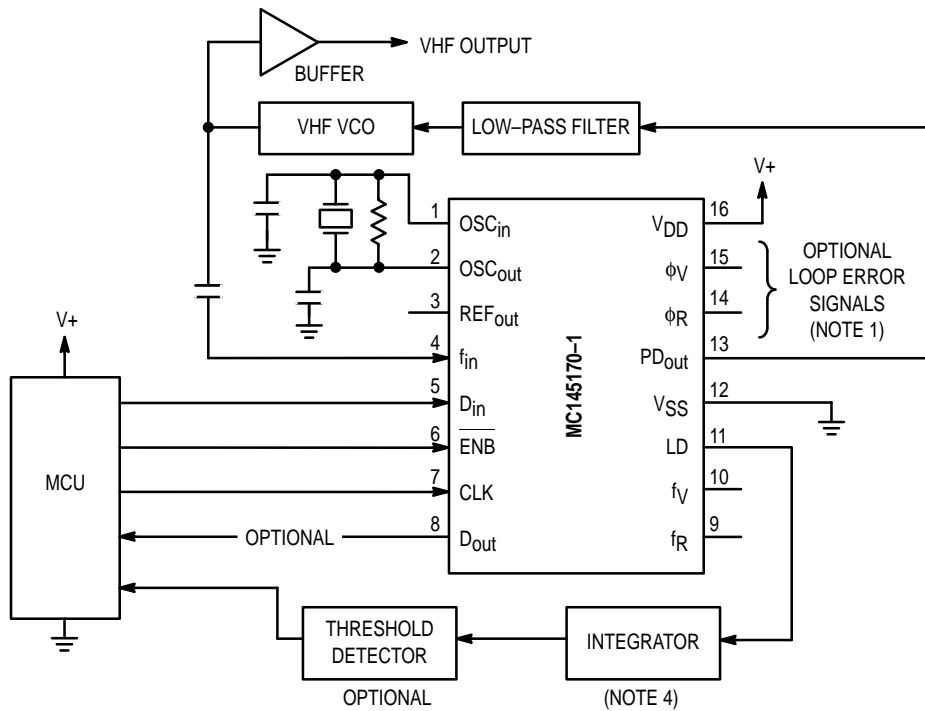
$$K_{VCO} \text{ (VCO Gain)} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor  $\zeta \approx 0.7$  and a natural loop frequency  $\omega_n \approx (2\pi f_R / 50)$  where  $f_R$  is the frequency at the phase detector input. Larger  $\omega_n$  values result in faster loop lock times and, for similar sideband filtering, higher  $f_R$ -related VCO sidebands.

**RECOMMENDED READING:**

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.  
 Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.  
 Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.  
 Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.  
 Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.  
 Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.  
 Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.  
 Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538-586. New York, John Wiley & Sons.  
 Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN*. March 5, 1980.  
 AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.  
 AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design*, 1987.  
 AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.

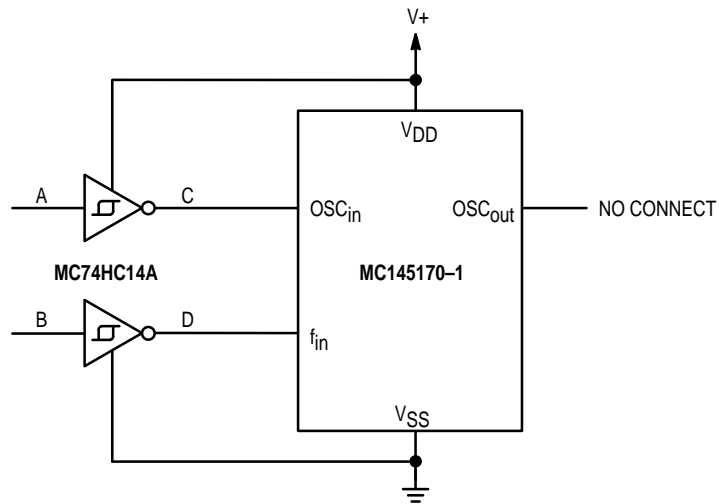




NOTES:

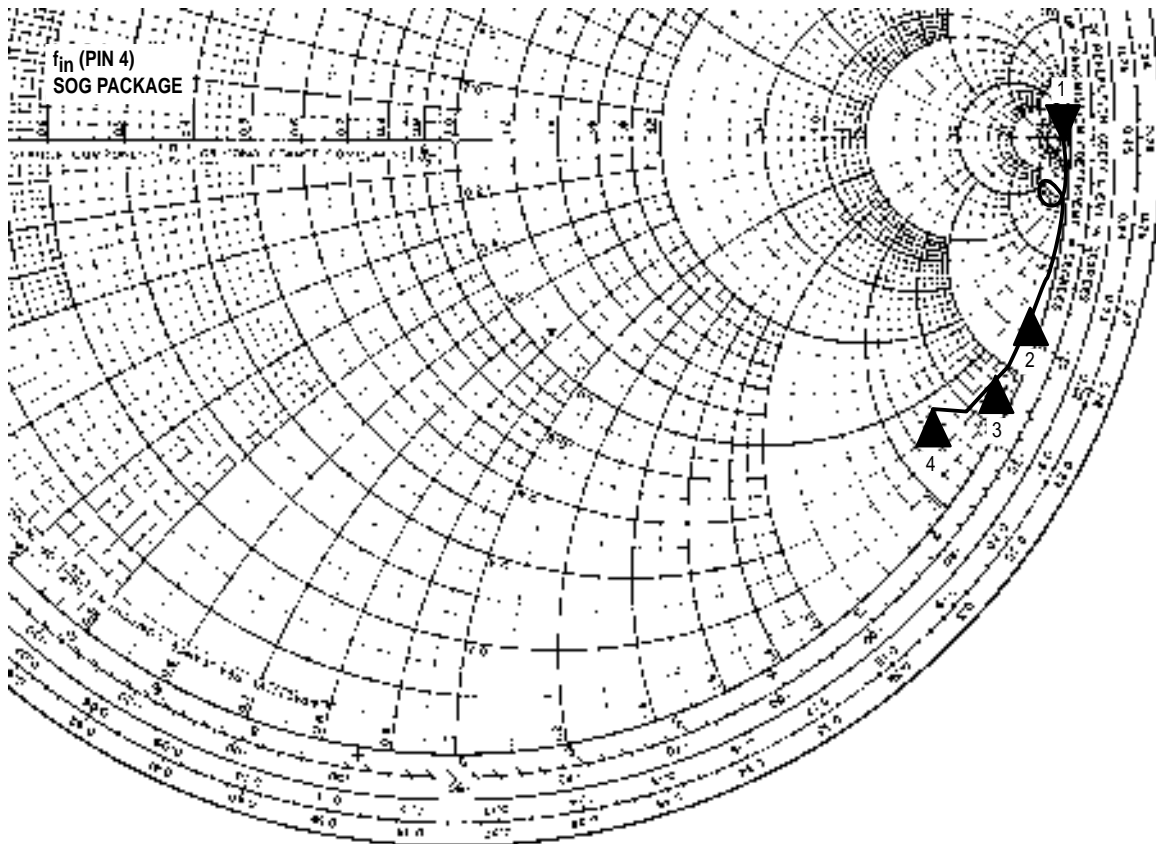
1. The  $\phi_R$  and  $\phi_V$  outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information. The  $\phi_R$  and  $\phi_V$  outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the  $V_{DD}$  pin to  $V_{SS}$  (GND) with one or more low-inductance capacitors.
3. The R counter is programmed for a divide value =  $OSC_{in}/f_R$ . Typically,  $f_R$  is the tuning resolution required for the VCO. Also, the VCO frequency divided by  $f_R = N$ , where N is the divide value of the N counter.
4. May be an R-C low-pass filter.

Figure 21. Example Application



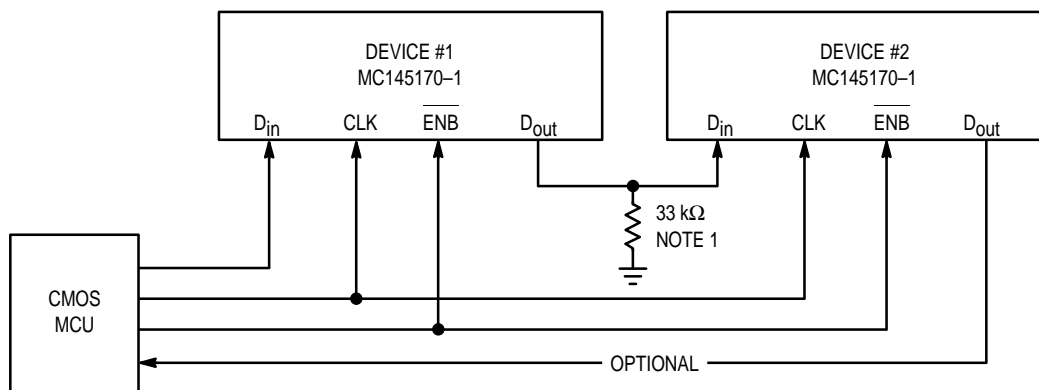
NOTE: The signals at Points A and B may be low-frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail-to-rail signal swings. With signals as described at Points C and D, the MC145170-1 is guaranteed to operate down to a frequency as low as dc.

**Figure 22. Low Frequency Operation Using dc Coupling**



Marker	Frequency (MHz)	Resistance ( $\Omega$ )	Reactance ( $\Omega$ )	Capacitance (pF)
1	5	2390	-5900	5.39
2	100	39.2	-347	4.58
3	150	25.8	-237	4.48
4	185	42.6	-180	4.79

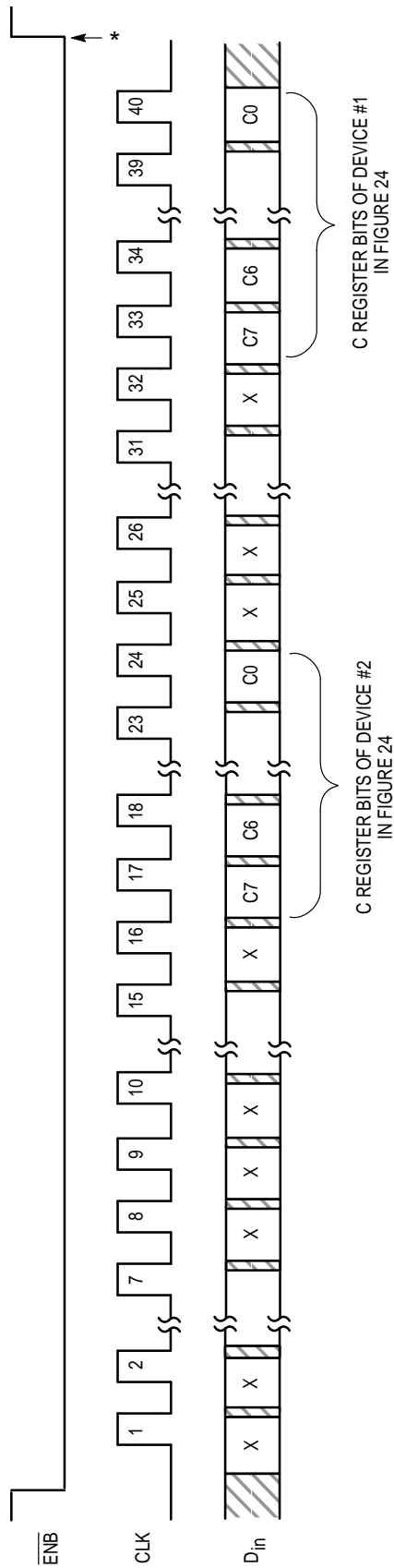
Figure 23. Input Impedance at  $f_{in}$  — Series Format ( $R + jX$ )  
(5 MHz to 185 MHz)



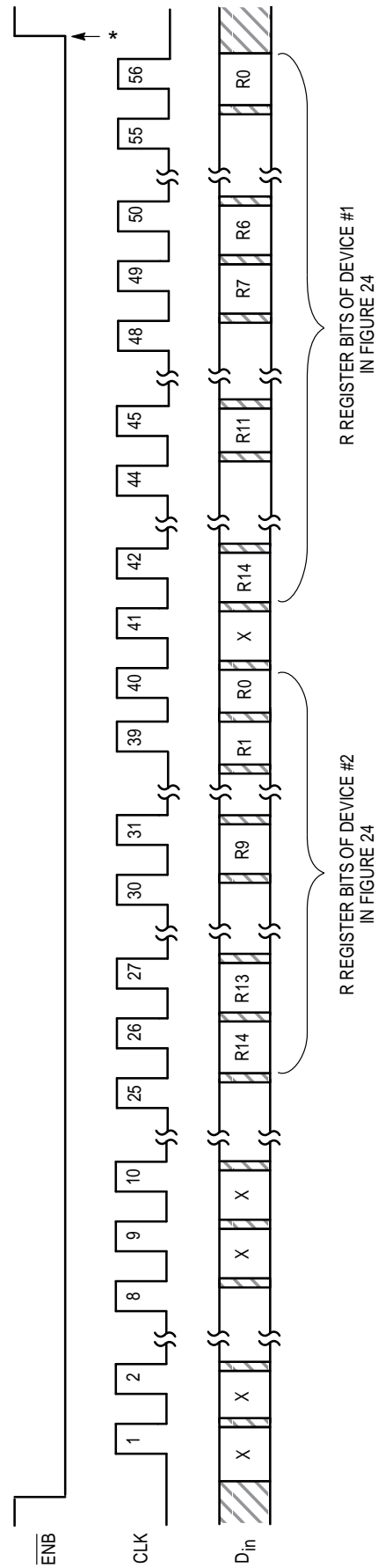
NOTES:

1. The 33 k $\Omega$  resistor is needed to prevent the  $D_{in}$  pin from floating. (The  $D_{out}$  pin is a three-state output.)
2. See related Figures 25, 26, and 27.

Figure 24. Cascading Two MC145170-1 Devices



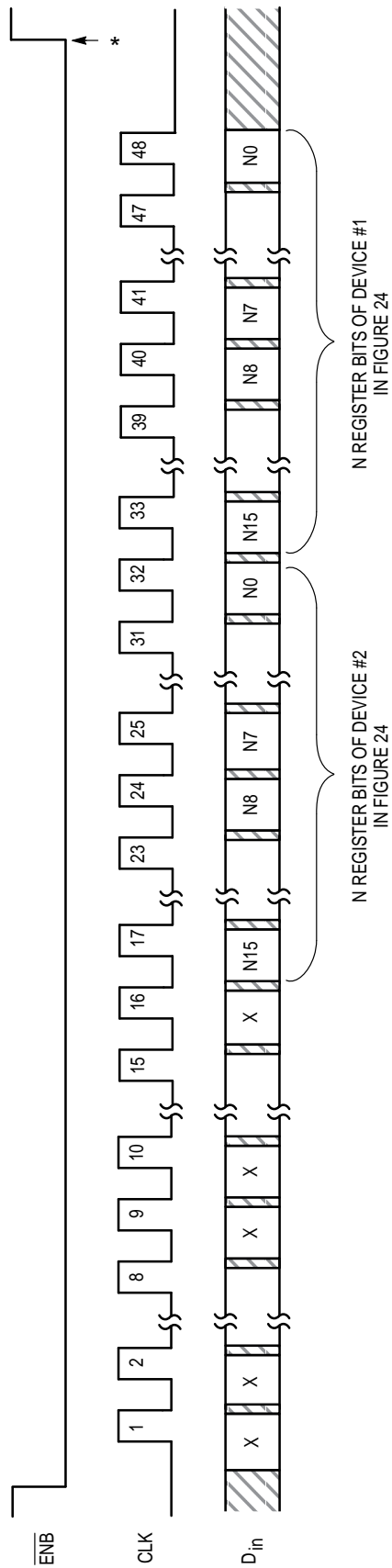
\*At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.



\*At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.

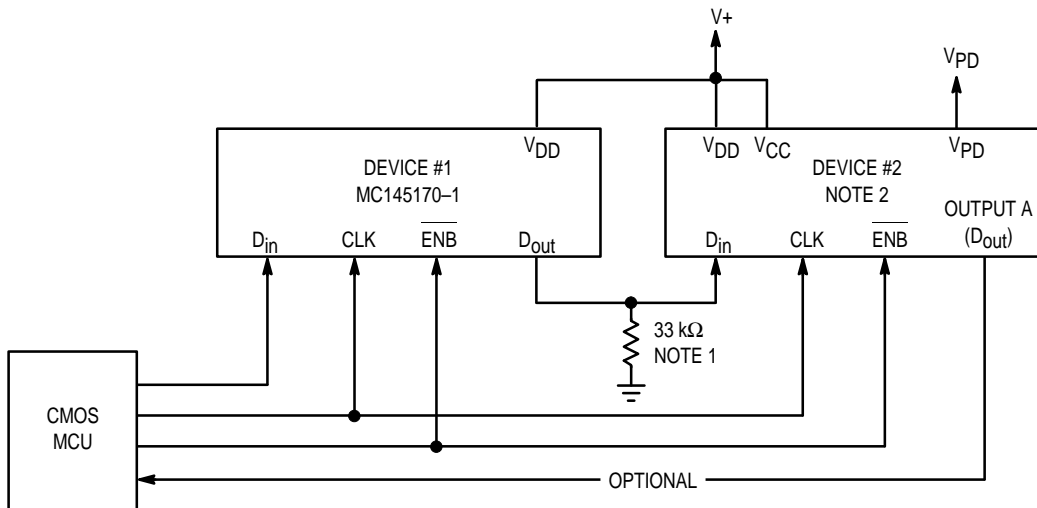
Figure 25. Accessing the C Registers of Two Cascaded MC145170-1 Devices

Figure 26. Accessing the R Registers of Two Cascaded MC145170-1 Devices



\*At this point, the new data is transferred to the N registers of both devices and stored. No other registers are affected.

Figure 27. Accessing the N Registers of Two Cascaded MC145170-1 Devices



NOTES:

1. The 33 kΩ resistor is needed to prevent the D<sub>in</sub> pin from floating. (The D<sub>out</sub> pin is a three-state output.)
2. This PLL Frequency Synthesizer may be a MC145190, MC145191, MC145192, MC145200, or MC145201.
3. See related Figures 29, 30, and 31.

**Figure 28. Cascading Two Different Device Types**

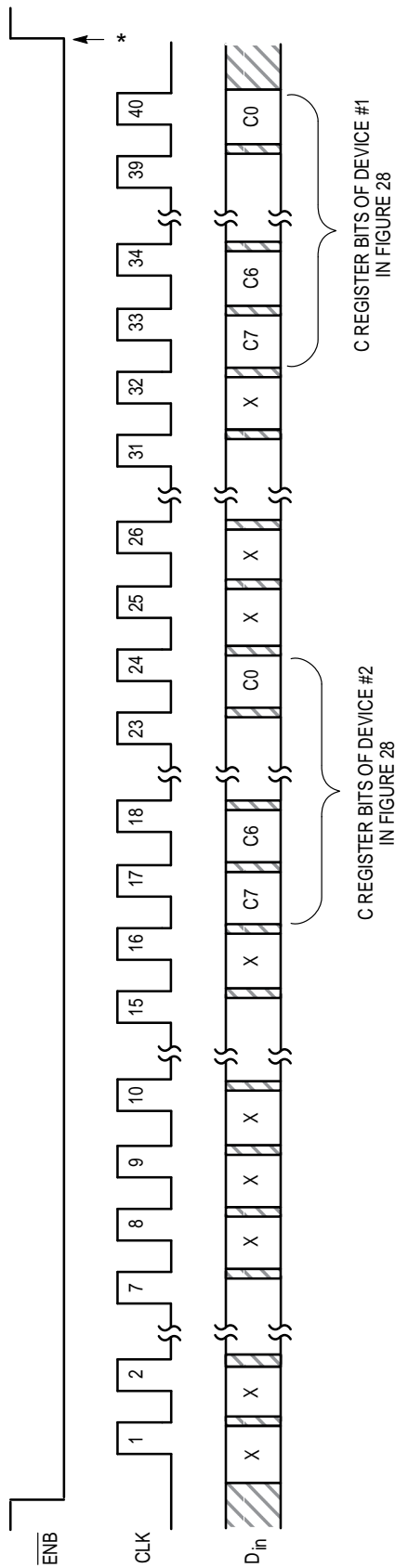


Figure 29. Accessing the C Registers of Two Different Device Types

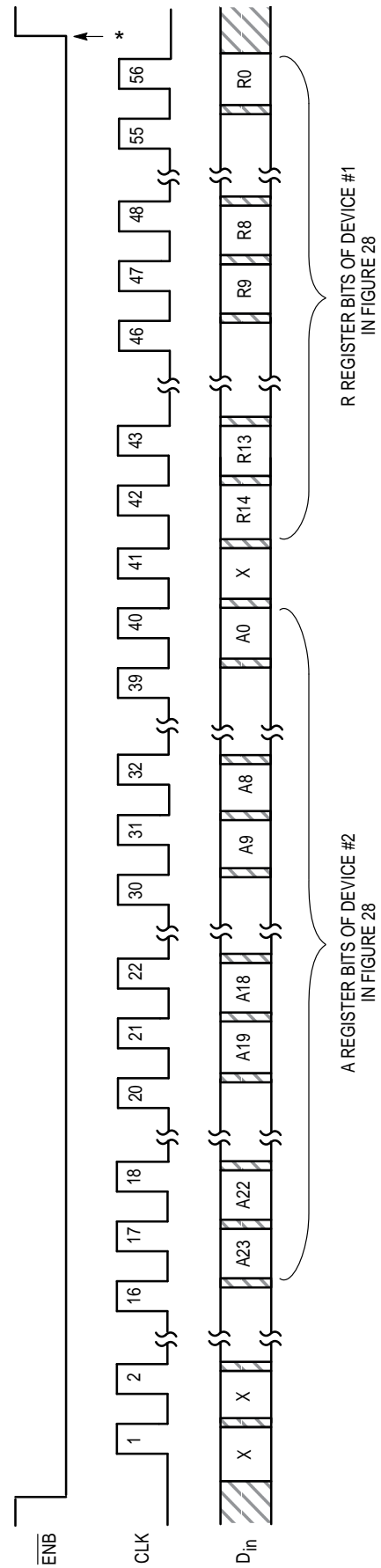
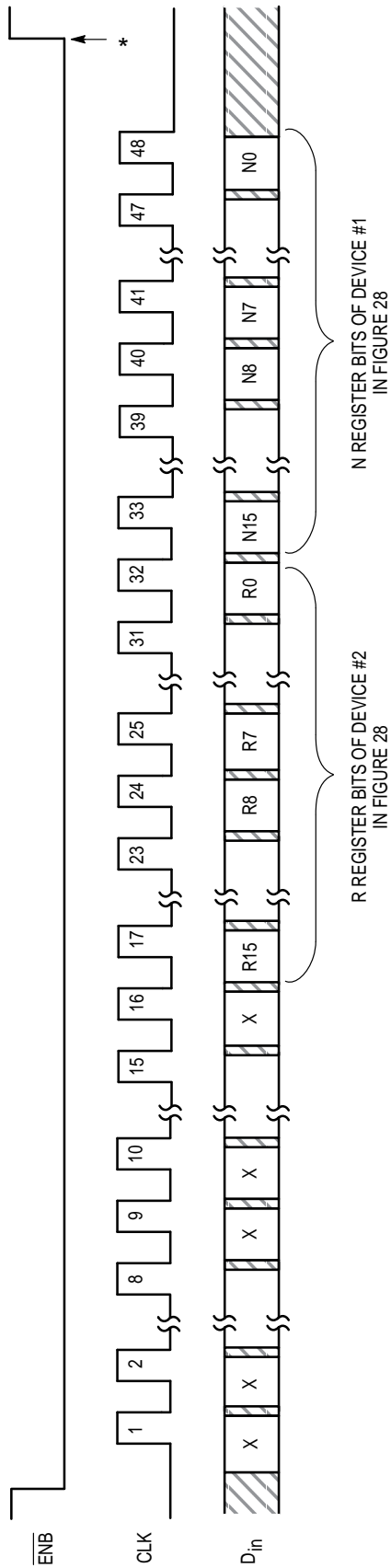


Figure 30. Accessing the A and R Registers of Two Different Device Types



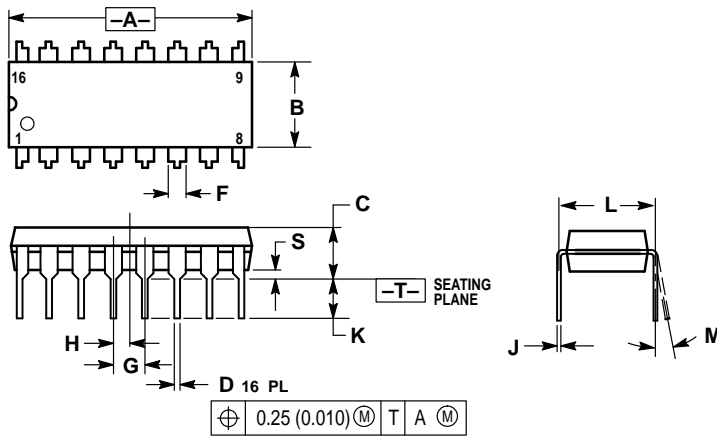
\*At this point, the new data is transferred to the R register of Device #2 and N register of Device #1 and stored. No other registers are affected.

**Figure 31. Accessing the R and N Registers of Two Different Device Types**



## PACKAGE DIMENSIONS

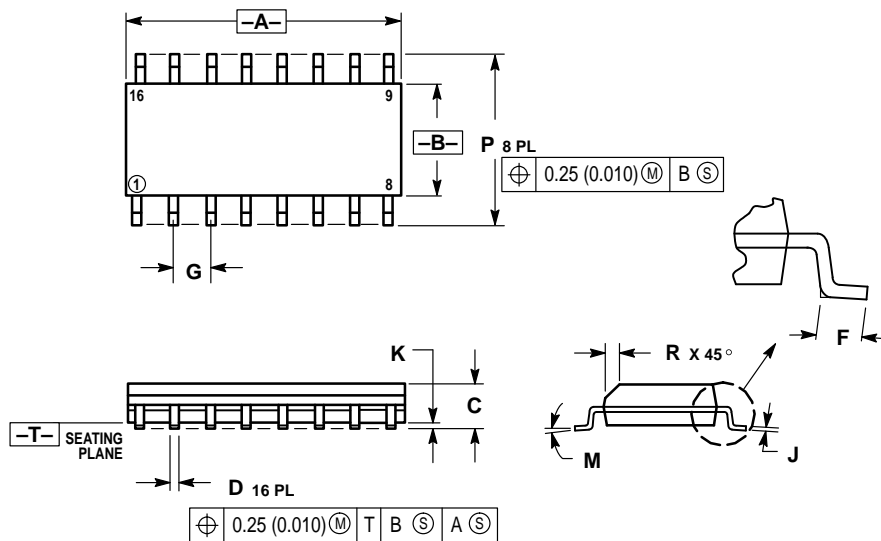
### P SUFFIX PLASTIC DIP (DUAL-IN-LINE PACKAGE) CASE 648-08



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

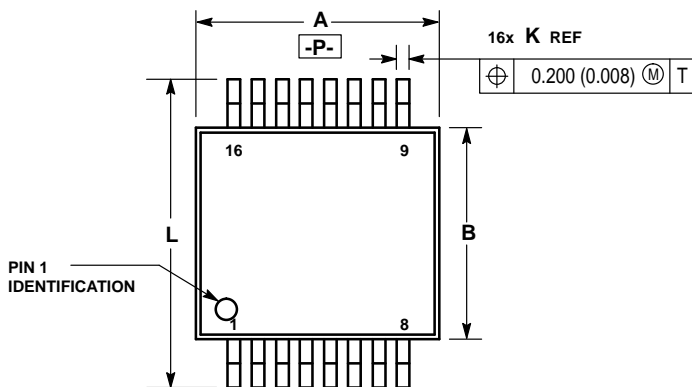
### D SUFFIX SOG (SMALL-OUTLINE GULL-WING) PACKAGE CASE 751B-05



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

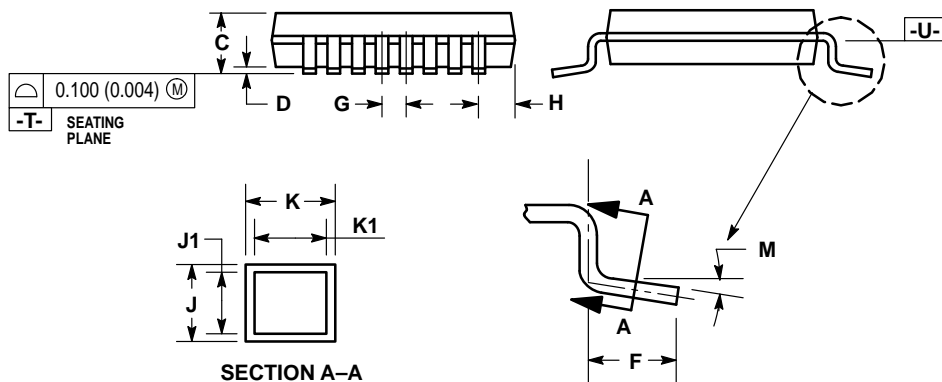
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

**DT SUFFIX**  
**TSSOP (THIN SHRUNK SMALL-OUTLINE PACKAGE)**  
**CASE 948C-03**




**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -U-.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	5.10	—	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0° 10°		0° 10°	

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